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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,381	12/16/2005	Shafidul Islam	102423-108	9287

27267 7590 09/17/2008

WIGGIN AND DANA LLP
ATTENTION: PATENT DOCKETING
ONE CENTURY TOWER, P.O. BOX 1832
NEW HAVEN, CT 06508-1832

EXAMINER	
YEUNG LOPEZ, FEIFEI	
ART UNIT	PAPER NUMBER
2826	
MAIL DATE	DELIVERY MODE
09/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,381	ISLAM ET AL.	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

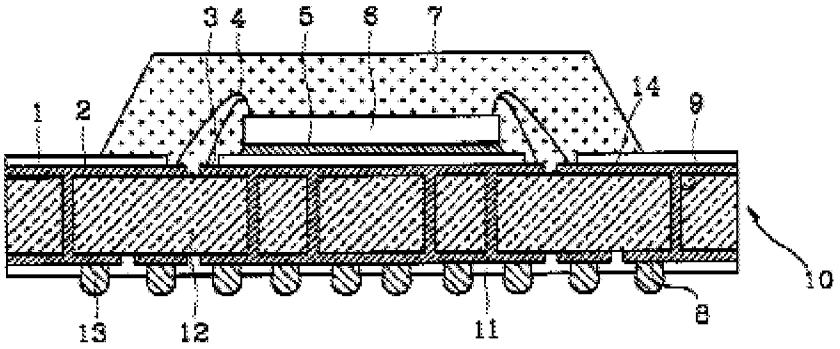
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-5 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (PG Pub 2002/0105077 A1) in view of Kuo et al (PG Pub 2002/0197842 A1).

4. Regarding claim 1, Choi teaches a package for encasing at least one semiconductor device, comprising: a lead frame (e.g. layer 14 in fig. 1) having opposing first and second ends, said first ends of said lead frame terminating in an array of lands (portions of layer 2 under layer 9 on the left and right of fig. 1) adapted to be bonded to external circuitry (solder balls 13) and said second ends terminating at an array of chip attach sites (layer 2) that are electrically interconnected to input/output pads on said at least one semiconductor device (through wires 4); a plurality of electrically isolated routing circuits (layer 9) electrically interconnecting individual combinations of said array

of lands and said array of chip attach sites; a first molding compound (layer 11) disposed between individual lands of said array of lands; and a second molding compound (layers 7 and 12) encapsulating said at least one semiconductor device, said array of chip attach sites and said routing circuits. However, Choi does not teach that the array of chip attach sites are directly electrically interconnected to input/output pads on said semiconductor device. In the same field of endeavor, Kuo teaches a flip chip for the benefit of providing a better performance device (paragraph [0004]). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a flip chip as the semiconductor device for the benefit of providing a better performance device. Note that the combined teaching of Choi and Kuo meets the claimed limitation that the array of chip attach sites are directly electrically interconnected to input/output pads on said semiconductor device.

FIG. 1 (PRIOR ART)



5. Regarding claim 2, Choi teaches the package of claim 1 wherein said lead frame and said routing circuits are elements of a single electrically conductive substrate (substrate 10 in fig. 1).

6. Regarding claim 3, Choi teaches the package of claim 2 wherein said single electrically conductive substrate is copper (paragraph [0008]).

7. Regarding claim 4, Choi teaches the package of claim 2 wherein a first perimeter defined by said array of lands (layers 2 is within the left and right borders of chip6, see fig. 3) does not exceed a second perimeter defined by said at least one semiconductor device.

8. Regarding claim 5, Choi teaches the package of claim 4 being a chip scale package (see fig. 1).

9. Regarding claim 9, Choi teaches the package of claim 2 further including a die pad (layer 3 in fig. 1) for bonding one of said at least one semiconductor devices, said die pad being monolithic with said lead frame.

10. Regarding claim 10, Choi teaches the package of claim 2 further including bond sites for bonding a passive device (elements 13 in fig. 1), said bond sites being monolithic with said lead frame.

11. Regarding claim 11, Choi teaches the package of claim 2 wherein said array of lands (layers 2 on the left and right under layer 9 in fig. 1) and said first molding compound (layer 11) are coplanar.

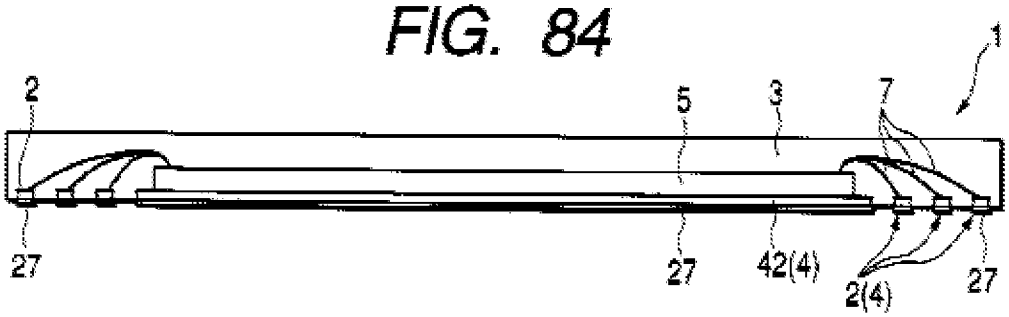
12. Regarding claim 12, Choi teaches the package of claim 2 wherein said array of lands (layers 2 on the left and right under layer 9 in fig. 1) extend beyond said first

molding compound (portions of layer 2 contacting areas indicated 8 and 13 exceed the leftmost and on the rightmost portions of layer 11 under substrate 10 and to the right of portions indicated 8 and 13, respectively, see fig. 1).

13. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over over Choi (PG Pub 2002/0105077 A1) in view of Kuo et al (PG Pub 2002/0197842 A1) as applied to claim 2 above, and further in view of Shimanuki et al (PG Pub 2002/0168796 A1).

14. Regarding claim 6, the previous combination remains as applied in claim 2. However, the previous combination does not teach that a distance between said at least one semiconductor device and said muting circuits is at least 75 microns. In the same field of endeavor, Shimanuki teaches a distance (the thickness of layer 4 in fig. 84) between at least one semiconductor device (layer 5) and a routing circuits (layer 27) is at least 75 microns (see paragraph [0187]). Choi also teaches that a space defined by said distance is filled with said second molding compound (layer 12 in fig. 1). Also note that discovery of an optimum range is well within the level of ordinary skill in the art, and such ranges will not support patentability unless there is evidence of its criticality. In re Aler, 220 F.2d 454.456.

FIG. 84



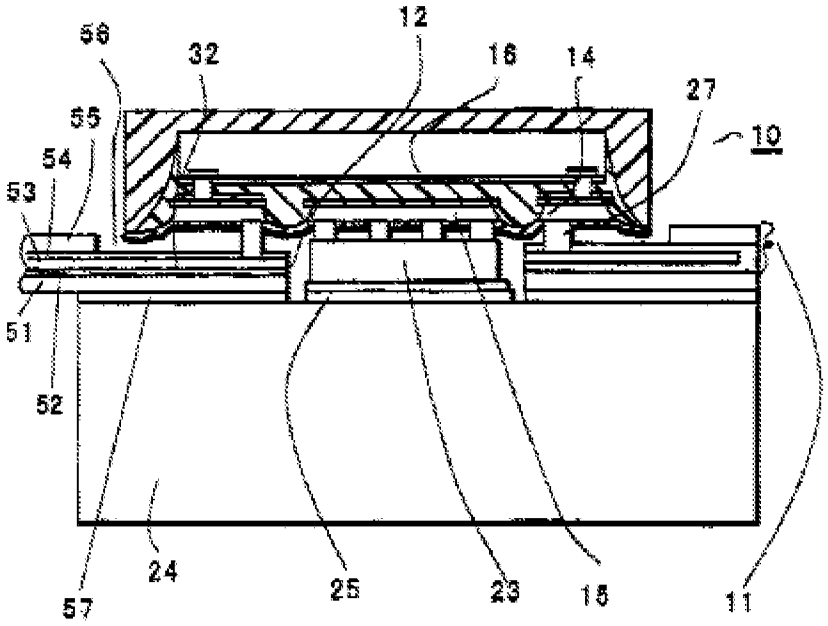
15. Regarding claim 7, Shimanuki teaches said distance is from 100 microns to 150 microns (0.15 mm, see paragraph [0187]).

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (PG Pub 2002/0105077 A1) in view of Kuo et al (PG Pub 2002/0197842 A1) as applied to claim 2 above, and further in view of Sakamoto et al (US Patent 6,967,401 B2).

17. Regarding claim 8, the previous combination remains as applied in claim 2. However, the previous combination does not teach a heat sink that is a single electrically conductive substrate with said lead frame and coplanar with said array of lands. In the same field of endeavor, Sakamoto teaches a heat sink (layer 15 in fig. 1B) that is coplanar with an array of lands (elements under layer 15 in fig. 1B) for the benefit of dissipating heat from a semiconductor device (abstract). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a heat sink under layer 9 and between layers 9 and 2 in fig. 1 of Choi's that is coplanar with the array of lands for the benefit of dissipating heat from the semiconductor device. Note that the combined teaching of Choi and Sakamoto meet the claimed limitation that the

heat sink is a single electrically conductive substrate with a lead frame since it is attached to layer 2 and sealed by layer 11 in fig. 1 of Choi's.

FIG.1B



Response to Arguments

18. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/
Primary Examiner, Art Unit 2826

FYL

/Feifei Yeung-Lopez/
Examiner, Art Unit 2826